

### Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 2, 10 and 11 have been amended. No claims have been canceled. Therefore, claims 1-29 are presented for examination.

Claims 1-29 stand rejected under 35 U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In the Office Final Office Action, the specification has been objected to because various ports shown in Figures 2-4 have not been described. Applicant submits that the specification has been amended to include a description of the ports in the Figures. Applicant submits that no new matter has been added since the ports were included in the Figures, and that one of ordinary skill in the art would have appreciated at the time the application was filed that the function of each of the previously non-described ports.

Claims 1-29 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the Examiner asserts that the term “data access primitive” used in the claims is not adequately described, nor enabled by the specification. See Office Final Action at page 4, paragraph 27.

Applicant submits that the present application is properly enabled. Data access primitives are described with reference to Figures 2, 3 and 4. In particular, the application describes that data access primitives are logic design components that may be used by a designer to specify an assembly of address and lane matching logic. Such logic is described in Figure 1. In addition, the Specification discloses that data access primitives hide the details of interconnection to a bus, and abstracts away the

interdependency of address-matching functions, lane-matching functions and data bus connections. See Specification at page 7, lines 4-10.

Moreover, the Specification discloses that data access primitives are replaced by a data access technology mapper with low level logic components in order to implement the address-matching functions, lane-matching functions and data bus connections. Id. At page 9, line 14 – page 11, line 5. Therefore, applicant submits that the element “data access primitive has been adequately defined in the Specification.

In addition, the Examiner maintains that the Specification does not adequately define “converting”. See Final Office Action at Page 5, paragraph 31. Applicant submits that this objection has been obviated by the amendment of the claims. Accordingly, the present claims are properly enabled.

Claims 1-29 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claims the subject matter which application regards as invention. Particularly, the Examiner asserts that the term “data access primitive” used in the claims is not adequately defined in the specification.

As discussed above with respect to the rejection under 35 U.S.C. § 112, second paragraph, applicant submits that “data access primitive” is adequately defined in the Specification. As discussed above, data access primitives are described as logic design components that may be used by a designer to specify an assembly of address and lane matching logic. Further, each data access primitive implies address-matching functions, lane-matching functions, data bus connections for one or more bytes of data and auxiliary logic. See Specification at page 7, lines 4-15. Therefore, the term “data access primitive” is properly defined in the Specification.

Further, the Examiner has interpreted the term “data access primitive” according to various definitions. Applicant has expressly denied such interpretations in a previous response. For instance, applicant has, and continues to, maintain that “data access primitive” be interpreted as described in the Specification.

Claims 1-4, 6-13, 15-18, 20-24, and 26-29 stand rejected under 35 U.S.C. §102(b) as being anticipated by Advanced Microprocessors of Tabak ("Tabak"). Applicant submits that the present claims are patentable over Tabak.

Tabak discloses various microprocessor architectures. However, claim 1 of the present application recites replacing a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device based upon the data access primitive and a first starting address. Applicant submits that nowhere in Tabak is there disclosed a data access primitive as recited in claim 1. As discussed above, applicant denies any interpretation of a data access primitive other than as described in the Specification.

Moreover, there is no disclosure of replacing such a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device. Accordingly, claim 1 is patentable over Tabak. Claims 2-9 depend from claim 1 and include additional limitations. Thus, claims 2-9 are also patentable over Tabak.

Claim 10 recites replacing a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device based upon the data access primitive and a first starting address. Thus, for the reasons described above with respect to claim 1, claim 10 is also patentable over Tabak. Because claims 11-17 depend from claim 10 and include additional limitations, claims 11-17 are also patentable over Tabak.

Claim 18 recites generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections. There is no disclosure in Tabak of generating logic components that implement address matching and lane matching functions, or one or more bus connections. Therefore, claim 18 is also patentable over

Tabak. Since claims 19-23 depend from claim 18 and include additional limitations, claims 19-23 are also patentable over Tabak.

Claim 24 recites generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections. Thus, for the reasons described above with respect to claim 18, claim 24 is also patentable over Tabak. Since claims 25-29 depend from claim 24 and include additional limitations, claims 25-29 are also patentable over Tabak.

Claims 5, 14, 19, and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tabak in view of applicant's admission. Applicant submits that the present claims are patentable over Tabak even in view of background of the application.

Applicant's background discloses specifying the addressability and bus connections, and the tediousness of a designer to explicitly specify designing for 8-bit and 32-bit system busses. See Specification at pages 1 and 2. However, if anything, applicant's background teaches away from the claims since the claims recite generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

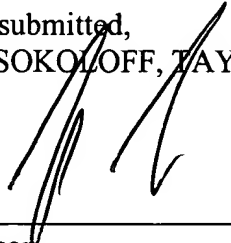
As described above, Tabak does not disclose or suggest such a limitation. Therefore, the present claims are patentable over any combination of Tabak and applicant's background since neither disclose nor suggest generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,  
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